REMARKS/ARGUMENTS

Claims 1-23 are currently pending in the present patent application.

In Section 4 of the Office Action mailed July 23, 2008, the Examiner maintains the rejection of claims 1-23 under 35 U.S.C. § 101 as being directed to nonstatutory subject matter.

Under Section 9a of the Office Action the Examiner responds to the undersigned's prior arguments regarding this rejection and states that the claims are rejected for two reasons: "[1] without disclosing a practical/physical application [;]and [2] preemption". The Examiner states that "there is no architecture or how the data is distributed among the processors in the multi-cores/processors as alleged by the applicant. . ." The Examiner also states that "all the claims, particularly independent claims, are cited so broad that they merely cover two steps butterfly computations and distributing the computations among processors which are seen in almost FFT/IFFT computations in multi-cores/processors. Thus, the claims 1-23 appear to preempt every substantial practical application of the idea embodied within the claims by just computing a number of butterfly stages and distributing among processors. There is nothing in the claims that would specifically direct to a method of controlling a multiprocessor system as alleged by the applicant."

Under Section 9b of the Office Action the Examiner responds to the undersigned's prior arguments regarding this rejection and states that "the alleged limitations 'the communications among the PEs happens only after log2(P) stages and only once for the rest of the FFT computation' might be seen in Figures 2-3, but not directly seen in the claim 1. Claim 1, based on the claim language, does not disclose any direct communications among the PEs ONLY after log2(P) stages and ONLY once for the rest of the FFT computation . . . Thus, the Examiner does not need to address/show this alleged limitations in the primary reference."

Amended claim 1 recites a method for controlling processing elements in a multiprocessor architecture to provide improved throughput for FFT/IFFT

computations. The method includes the steps of computing, on a multiprocessor architecture including "P" processing elements, each butterfly of the first "$\log_2 P$" stages of an FFT/IFFT on either a single one of the processing elements or on each of the "P" processing elements simultaneously. The method further includes distributing the computations of the butterflies in all the subsequent stages of the FFT/IFFT among the "P" processing elements such that each chain of cascaded butterflies consisting of those butterflies that have inputs and outputs connected together are processed by the same processing element to thereby eliminate the need for inter-processor communication among the processing elements after the computation of the first "$\log_2 P$" stages of the FFT/IFFT.

Amended claim 1 now expressly recites a method for controlling processing elements in a multiprocessor architecture to provide improved throughput for FFT/IFFT computations that includes the recited operations of computing and distributing. This recited method certainly recites patentable subject matter, whether under the "machine-or-transformation" test recently elucidated by the Federal Circuit *en banc* in *In re Bilski*, Fed. Cir., No. 2007-1130, 30 October 2008, or under the prior seeming variations or alternative phrasing of this test discussed therein.

Under Bilski, the threshold question in determining whether a claim recites patent eligible subject matter is whether the claim recites a fundamental principle and, if so, whether the claim would pre-empt substantially all uses of that fundamental principle. See Bilski, p. 10. In Bilski the Federal Circuit defines a fundamental principle as a law of nature, natural phenomena, or abstract idea. A mathematical algorithm alone is not patentable as being akin to either a law of nature or an abstract idea. But a mathematical algorithm may certainly be part of a patent-eligible claim, as was the case with the patent-curing process including the Arrhenius equation at issue in *Diamond v. Diehr*, 450 U.S. 175 (1981).

Claim 1 and the other independent claims of the present application certainly relate to fast Fourier transforms (FFTs) and inverse FFTs and therefore for the

purposes of the following discussions are assumed to recite a fundamental principle. The question then becomes whether the claims pre-empt the use of FFT/IFFT algorithms. The present claims simply do not pre-empt the use of performing FFT or IFFT algorithms. There are an infinite number of ways of performing calculations for such FFT and IFFT algorithms and the present claims merely relate to one way of calculating these algorithms in which certain computations and distribution of computational results are performed as recited in the independent claims.

Bilski explains that a claimed process does not pre-empt substantially all uses of a recited fundamental principle if the process is 1) tied to a machine or 2) transforms an article into a different state or thing. All independent claims also satisfy both prongs of this two-pronged inquiry, evidencing the conclusion just discussed above that the claims do not pre-empt the use of the FFT or IFFT algorithm. With regard to the first prong, amended claim 1 recites a method for controlling processing elements in a multiprocessor architecture to provide improved throughput for FFT/IFFT computations that includes the steps of "computing, on a multiprocessor architecture including "P" processing elements, each butterfly of the first "$\log_2 P$" stages of an FFT/IFFT ..." and "distributing the computations of the butterflies in all the subsequent stages of the FFT/IFFT among the "P" processing elements ...." The recited method is accordingly tied to a machine, namely a multiprocessor architecture including P processing elements. The process is not merely tied to a general purpose computer but instead is tied to the specific machine having a multiprocessor architecture including P processing elements. Thus, this claim is tied to a specific machine and accordingly does not pre-empt all uses of the recited FFT/IFFT.

Claim 1 also satisfies the second prong of the Bilski two-part test in that the recited process transforms an article into a different state or thing. The article, which in this case corresponds to samples of an input data signal in first domain, such as the time domain ("index n is often associated with time," see paragraph 4), are transformed into a second domain, such as the frequency domain ("k denoting frequency," see paragraph 4). As noted by the Federal Circuit in Bilski, "the mere fact

that a claimed invention involves inputting numbers, calculating numbers, outputting numbers, and storing numbers, in and of itself, would not render it nonstatutory subject matter." See Bilski, pp. 23 quoting *AT&T Corp. v. Excel Commc'ns, Inc*, 172 F.3d 1352 (Fed Cir. 1998). Claim 1 recites a particular way of controlling the recited processing elements P to transform data from one domain to another domain and, accordingly, recites patent-eligible subject matter. The process covers distributing the data among the processing elements to achieve the recited functionality.

Amended claim 9 recites a method of performing a fast Fourier transform or inverse fast Fourier transform on an input signal. The method includes storing samples of the input signal in a memory and retrieving the samples from the memory. From these retrieved samples the method includes calculating the butterfly computational blocks for the first $\log_2 P$ stages of the transform on a single processor or on a plurality of processors operating in parallel. The method further includes eliminating the need for communication among and between the processors after the computation of the first "$\log_2 P$" stages of the transform by calculating chains of butterfly computational blocks corresponding to the subsequent stages of the transform within each of the processors. Each chain of butterfly computational blocks that is calculated in a respective processor has inputs and outputs coupled in series.

Once again, claim 9 does not pre-empt substantially all uses of this algorithm and satisfies both prongs of the two-part machine-or-transformation test set forth in Bilski. The recited method is tied to a machine, namely the recited memory in which the samples of the input signal are stored and the recited plurality of processors. Moreover, the method transforms the samples of the input signal in one domain into corresponding data in another domain via the recited FFT/IFFT transform. Not all uses of this transform are pre-empted via the claim, however, with quite the contrary being true. The claim pre-empts only the specific approach of calculating the transform as is recited in the claim by performing the butterfly calculations within the processors as set forth in the claim.

Amended claims 5, 16 and 21 are not method claims but instead are apparatus claims and so certainly are directed to patent-eligible subject matter under Section 101. Moreover, the rationale discussed above with regard to claim 1 applies these claims as well insofar as pre-emption of the recited FFT/IFFT algorithm is concerned. These claims are, simply put, directed to particular machines and accordingly are directed to a statutory class of subject matter under Section 101 (i.e., these claims recite patent-eligible subject matter).

For all these reasons, independent claims 1, 5, 9, 16 and 21 are directed to patent-eligible subject matter under Section 101 and the rejections of these claims under this section should be withdrawn.

Finally, in Sections 5 and 6 of the Office Action the Examiner maintains his rejections of claims 1-2, 9-10, 16-17, and 20-23 under 35 U.S.C. § 102(b) as being anticipated by the paper entitled "Performance Analysis of FFT Algorithms on Multiprocessor Systems" to Laxmi *et al.* ("Laxmi"). In Sections 7 and 8 the Examiner maintains his rejections of claims 11-13 under 35 U.S.C. § 103(a) as being unpatentable over Laxmi.

Amended claim 1 now expressly recites that the first $\log_2 P$ stages of butterfly calculations are performed as recited and in combination with the limitation that the butterfly calculations of all subsequent stages are distributed so that inter-processor communication is eliminated for all these subsequent stage calculations. None of the prior art cited by the Examiner alone or in combination discloses or suggests these recited operations. Specifically, in Laxmi the processing elements start to communicate with each other after $\log_2 N/P$ stages (see pp. 513, right column, section II, "Radix-2 FFT Computation"), where N is the length the data sequence or number of points or samples being processed via the algorithm and P is the number of processing elements PE. Laxmi simply does not disclose eliminating communication among processing elements after $\log_2 P$ stages. In contrast, with the computing and distributing operations recited in claim 1 communications among the processing

elements happens after $\log_2 P$ stages and only once for the rest of the FFT/IFFT computation as is evident from the embodiments of the invention covered by claim 1 and depicted in Figures 2 and Figure 3 of the present application. For large FFTs/IFFTs (i.e., large number of points or samples) this greatly reduces the communication overhead associated performing the transformation.

For at least these reasons, the combination of elements recited in amended claim 1 is allowable. Dependent claims 2-4 are allowable for at least the same reasons as claim 1 and due to the additional limitations added by each of these dependent claims.

Amended independent claim 9 recites a method of performing a fast Fourier transform or inverse fast Fourier transform on an input signal. The method includes storing samples of the input signal in a memory, retrieving the samples from the memory and from these retrieved samples calculating the butterfly computational blocks for the first $\log_2 P$ stages of the transform on a single processor or on a plurality of processors operating in parallel. The method further includes eliminating the need for communication among and between the processors after the computation of the first "$\log_2 P$" stages of the transform by calculating chains of butterfly computational blocks corresponding to the subsequent stages of the transform within each of the processors, each chain of butterfly computational blocks that is calculated in a respective processor having inputs and outputs coupled in series.

Once again, as discussed above with reference to claim 1, Laxmi neither discloses nor suggests calculating butterfly computational blocks for the first $\log_2 P$ stages of the transform on a single processor or on a plurality of processors operating in parallel and eliminating the need for communication among and between the processors after the computation of the first "$\log_2 P$" stages. In contrast, with the approach of Laxmi the processing elements start to communicate with each other after $\log_2 N/P$ stages.

For at least these reasons, the combination of elements recited in amended claim 9 is allowable. Dependent claims 10-15 are allowable for at least the same reasons as claim 9 and due to the additional limitations added by each of these dependent claims.

Amended independent claim 16 recites a processor system including a memory operable to store samples of an input signal and a plurality of processors coupled to the memory. The plurality of processors are operable to receive the samples from the memory and to use the samples to execute the butterfly computational blocks for the first "$\log_2 P$" stages of a fast Fourier transform or inverse fast Fourier transform on either a single one of the processors or on a plurality of the processors operating in parallel. Address circuitry is coupled to the memory and processor and operable to distribute the computation of the butterfly computational blocks in all stages subsequent to the first $\log_2 P$ stages among the plurality of processors such that each chain of cascaded butterfly computational blocks in the transform are coupled in series and are computed by the same processor to thereby eliminate the need for communication among and between the processors after the computation of the first "$\log_2 P$" stages of the transform.

Laxmi neither discloses nor suggests a plurality of processors that execute the butterfly computational blocks for the first "$\log_2 P$" stages of a fast Fourier transform or inverse fast Fourier transform on either a single one of the processors or on a plurality of the processors operating in parallel and address circuitry that distributes the computation of the butterfly computational blocks in all stages subsequent to the first $\log_2 P$ stages among the plurality of processors such that each chain of cascaded butterfly computational blocks in the transform are coupled in series and are computed by the same processor. This eliminates the need for communication among and between the processors after the computation of the first "$\log_2 P$" stages of the transform.. In contrast, as already discussed above, with the approach of Laxmi the processing elements start to communicate with each other after $\log_2 N/P$ stages.

For at least these reasons, the combination of elements recited in amended claim 16 is allowable. Dependent claims 17-20 are allowable for at least the same reasons as claim 16 and due to the additional limitations added by each of these dependent claims.

Independent claim 21 is allowable for reasons similar to those discussed with reference to claim 16 and dependent claims 22-23 are allowable for at least the same reasons as claim 21 and due to the additional limitations added by each of these dependent claims.

In Sections 7 and 8 the Examiner maintains his rejections of claims 11-13 under 35 U.S.C. § 103(a) as being unpatentable over Laxmi. As discussed above with regard to independent claim 9, dependent claims 11-13 are allowable for at least the same reasons as independent claim 9 from which each of these dependent claims ultimately depends.

Claims 3-8, 14-15, and 18-19 are not rejected over any prior art in the Office Action but only under Section 101. Dependent claims 3-4, 14-15, and 18-19 are now allowable since, as discussed above, the independent claims from which they depend recite patent-eligible subject matter and are allowable over the art of record, as also discussed above.

Independent claim 5 is allowable for reasons similar to those discussed above with regard to independent claim 16. Furthermore, the Examiner has not shown that the art of record teaches or suggest, in combination with the other elements of claim 5, the elements of means for counting and means for computing twiddle factors for the butterfly computations at each processing elements, the means for computing initializing the means for counting and then incrementing the means for counting by a value corresponding to the number of processing elements "P" and appending the result with a specified number of "0"s.

For at least these reasons, the combination of elements recited in independent claim 5 is allowable. Dependent claims 6-8 are allowable for at least the same

reasons as claim 5 and due to the additional limitations added by each of these dependent claims.

For these reasons, the combination of elements recited in claim 1 is allowable and the remaining independent claims are allowable for reasons similar to claim 1. All dependent claims are allowable for at least the same reasons as the associated independent claim and due to the additional limitations added by each of these dependent claims.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. **Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to arrange for a telephone interview to discuss the outstanding issues.** If the need for any fee in addition to any fee paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

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